Attorney Docket No. 8836-223 (ID12244-US)

SEMICONDUCTOR MEMORY DEVICE TESTABLE WITH A SINGLE DATA RATE AND/OR DUAL DATA RATE PATTERN IN A MERGED DATA INPUT/OUTPUT PIN TEST MODE

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates to semiconductor memory devices and, more specifically, to semiconductor memory devices which are testable with a single data rate (SDR) and/or dual date rate (DDR) pattern in a merged data input/output pin (DQ) test mode.

2. Discussion of the Related Art

Testing semiconductor memory devices can be divided into two procedures when fabricating from raw wafers to completely packaged products. One procedure is a wafer test for detecting defects on a wafer where semiconductor chips have been manufactured. Another procedure is a package test for detecting defects in packaged products after the wafer test. Semiconductor products subject to these test procedures may typically be required to satisfy prior design specifications.

These design specifications tend to increase the number of input/output pins in semiconductor memory devices because of the need for higher capacities, integration densities, and facilities. Usually a test procedure is conducted by comparing actual data with expected (or desired) data by connecting the input/output pins of a semiconductor memory device

to the channels of a tester (or testing equipment). Based on the comparison result, one may determine whether or not there is a defect in the tested semiconductor memory device. Even though a large number of test channels are found in a typical tester, the increasing number of input/output pins in common semiconductor memory devices may reduce the number of semiconductor memory devices capable of being tested at one time by a tester. In addition, the increasing number of input/output pins relative to the limited number of test channels may increase test time for the semiconductor memory devices and thereby, increase the cost of the test and reduce the productivity of the tester.

In order to overcome the limited number of test channels in a tester versus the number of input/output pins in a semiconductor memory device, a merged DQ test scheme has been proposed. The merged DQ test scheme assigns the input/output pins (e.g., DQ pins) of a memory device to a single pin of a tester. Data bits to be output through a plurality of DQ pins are internally compared with each other (or an expected data bit), and then, as a single bit, the comparison result is output to the single pin of the tester. By unifying a plurality of DQ pins to a single test channel (or a single test pin) the number of semiconductor memory devices testable is increased and the test cost is reduced.

FIG. 1 illustrates an example of the merged DQ test scheme for use with a semiconductor memory device. A semiconductor memory device 100 to be tested is comprised of data latches 110, a data comparator 130, a data combiner 150, a merging controller 170, and output buffers 180 (including buffers 190-198). The data latches 110 hold internal data bits

I/O0-I/O8 of the memory device 100, in response to an internal clock signal KCORE. The internal data bits I/O0-I/O8 in the data latches 110 are transferred to the output buffers 180 through de-multiplexers DMUX during an inactive state of a merging signal MDQ and through the data comparator 130 during an active state of the merging signal MDQ. In a normal operation mode, not a test mode, the output buffers 180 output the latched data bits I/O0-I/O8 through DQ pads (DQ0-DQ8) (or pins).

In a merged DQ test mode, the data comparator 130 compares the latched data bits I/O0-I/O8 to each other and then transfers the comparison results to the data combiner 150. In the data combiner 150, the comparison results are put into an exclusive-OR (XOR) logic circuit and an output of the XOR logic circuit is applied to the merging controller 170 as an output DOUTMDQB in response to the merging signal MDQ. The merging controller 170 transfers its own output DOUTMDQ to one of the output buffers 190-198, e.g., output buffer 195, in response to an output clock signal KDATA and a merging flag signal MFLAG. An output from the output buffer 195 is transmitted to its corresponding DQ pad DQ5 by control of an output enable generator that responds to the merging signal MDQ and provides an output enable signal to permit data to be output to the output buffer's 195 DQ pad DQ5. Therefore, the DQ pad DQ5 selected as an output terminal for the merged data bit becomes a merged DQ pad in the merged DQ test mode.

The data combiner 150 generates two outputs: one is a first merging data bit DOUTMDQB_W that is active at a rising edge of the clock signal; the other is a second merging data bit DOUTMDQB_X that is active at a

falling edge of the clock signal. Referring to FIG. 2, which shows a circuit diagram of the merging controller shown in FIG.1, in the merging controller 170, the first and second merging data bits, DOUTMDQB_W and DOUTMDQB_X, alternatively trigger the output DOUTMDQ in response to output clock signals KDATA_W1 and KDATA_X1, respectively when the merging flag signal MFLAG is active with a high level logically.

During this procedure, the output DOUTMDQ of the merging controller 170 is conductive in an SDR mode because the output clock signals KDATA_W1 and KDATA_X1 are not simultaneously enabled even though the merging data bits DOUTMDQB_W and DOUTMDQB_X are conductive in a DDR mode. Thus, the merging controller 170 does not operate in the DDR mode, rather it operates in the SDR mode while the data combiner 150 is operable in the DDR mode.

Therefore, the merged DQ test scheme with the merging controller shown in FIG. 2 is unavailable in the DDR mode required for high bandwidth synchronous semiconductor memory devices.

Summary of the Invention

It is, therefore, an object of the present invention to provide a semiconductor memory device having a merged data input/output pin (DQ) test function with a dual data rate (DDR) operation mode.

In accordance with the present invention, a semiconductor memory device operable in a merged DQ test mode, includes: a first path circuit; a second path circuit; and a merged output generator configured to generate a merged data bit having a single data rate (SDR) pattern and/or a dual data

rate pattern.

The semiconductor memory device further includes a control signal generator configured to generate a first and second SDR signal and a first and second transmission signal pair.

Brief Description of the Drawings

The forgoing features of the invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings, in which:

FIG. 1 is a circuit diagram illustrating an example of a merged data input/output pin (DQ) test mode in a semiconductor memory device;

FIG. 2 is a circuit diagram of the merging controller shown in FIG. 1;

FIG. 3 is a circuit diagram of a merging controller according to an exemplary embodiment of the present invention; and

FIG. 4 is a circuit diagram of a control signal generator according to an exemplary embodiment of the present invention.

Description of Exemplary Embodiments

FIG. 3 illustrates a circuit diagram of a merging controller according to an exemplary embodiment of the present invention. Referring to FIG. 3, a merging controller 300 includes a first path circuit 310, a second path circuit 330, and a merged output generator 350. The first path circuit 310 receives the first data bit DOUTMDQB_W and the merging flag signal MFLAG and then generates a first path output signal MDQ_W in response to a reset signal RESET, a second single data rate signal SDR_X, and a first

transmission signal pair W/WB. The second path circuit 330 receives the second data bit DOUTMDQB_X and the merging flag signal MFLAG and then generates a second path output signal MDQ_X in response to the reset signal RESET, a first single data rate signal SDR_W, and a second transmission signal pair X/XB. The merged output generator 350 receives the output signals MDQ_W and MDQ_X from the first and second path circuits 310 and 330 and generates the merged output data bit DOUTMDQ.

The first path circuit includes an inverter 312 receiving the merging flag signal MFLAG, a NOR gate 314 receiving an output of the inverter 312 and the first data bit DOUTMDQB_W, a transmission gate 316 switching an output of the NOR gate 314 in response to the first transmission signal pair W/WB, a PMOS transistor 318 controlled by the second single data rate signal SDR_X, a latch 320 retaining a current voltage level at a node NA, a second inverter 322 turning an output of the latch 320 to the output signal MDQ_W, an inverter 324 receiving the reset signal RESET, an inverter 326 receiving an output of the inverter 324, and an NMOS transistor 328 resetting the node NA in response to an output of the inverter 326. The second path circuit 330 is constructed similar to the first path circuit 310 and includes inverters 332, 342, 344, and 346, a NOR gate 334, a transmission gate 336, a PMOS transistor 338, a latch 340, and an NMOS transistor 348. The output signals of the first and second path circuits, MDQ_W and MDQ_X, are applied to the merged output generator 350. The merged output generator 350 includes a NAND gate 352 receiving the first and second path output signals, MDQ_W and MDQ_X, and an inverter 354 converting an output of the NAND gate 352 to the merged output data bit

DOUTMDQ.

A control signal generator 400 providing the first and second transmission signal pairs, W/WB and X/XB, and the first and second single data rate signals, SDR_W and SDR_X, is illustrated in FIG. 4. Referring to FIG. 4, the control signal generator 400 outputs the first and second transmission signal pairs, W/WB and X/XB, and the first and second single data rate signals, SDR_W and SDR_X, in response to output clock signals KDATAW0, KDATAW1, KDATAX0, and KDATAX1. The output clock signals KDATAW0, KDATAW1, KDATAX0, and KDATAX1 are activated in various combinational patterns according to a burst type and a current data rate mode (single data rate (SDR) and/or dual data rate (DDR)) as shown in the following Table 1.

[Table 1]

Burst Type	First	Second	Third	Fourth
Flag Address	00	01	10	11
DDR	KDATAW1 KDATAX0	KDATAW0 KDATAX1	KDATAW1 KDATAX0	KDATAW0 KDATAX1
SDR	KDATAW1 KDATAW0	KDATAX1 KDATAX0	KDATAW1 KDATAW0	KDATAX1 KDATAX0

As shown in Table 1, the flag address determines a burst type, among the first through fourth types, of a semiconductor memory device such as a DDR static random access memory (SRAM).

The control signal generator 400 includes a NOR gate 402 receiving the first and second output clock signals KDATAX0 and KDATAX1, inverters 404, 406, and 408 serially connected from an output of the NOR

gate 402, a NAND gate 410 outputting the second single data rate signal SDR_X, a NOR gate 412 receiving the third and fourth output clock signals KDATAW0 and KDATAW1, inverters 414, 416, and 418 serially connected from an output of the NOR gate 412, a NAND gate 420 outputting the first single data rate signal SDR_W. Outputs of the inverters 406 and 408 become the second complementary transmission signal pair XB and the second (i.e., main) transmission signal X respectively, and outputs of the inverters 416 and 418 become the first complementary transmission signal WB and the first (i.e., main) transmission signal W. The NAND gate 410 inputs the first complementary transmission signal WB and the second transmission signal X and then outputs the second single data rate signal SDR_X. The NAND gate 420 inputs the second complementary transmission signal XB and the first transmission signal W and then outputs the first single data rate signal SDR_W.

In the DDR mode with the first burst type, the second and third output clock signals, KDATAW1 and KDATAX0, are set to high levels. And, the first and second transmission signals W and X go to high levels (their complementary signals WB and XB are at low levels) while the first and second single data rate signals SDR_W and SDR_X are set to high levels.

In the SDR mode with the first burst type, the first and second output clock signals, KDATAW0 and KDATAW1, are set to high levels. And, the first and second transmission signals W and X go to high and low levels respectively (their complementary signals WB and XB are at low and high levels respectively) while the first and second single data rate signals SDR_W and SDR_X are set to low and high levels.

The merging controller 300 operates in a merged data input/output pin (DQ) test mode with the signals provided from the control signal generator 400. In the merged DQ test mode, the merging flag signal MFLAG is set to a high level.

In the DDR mode with the first burst type, the first and second single data rate signals SDR_W and SDR_X go to a high level to turn the PMOS transistors 318 and 338 off. During this, the first and second transmission signals, W and X, are at low levels and the transmission gates 316 and 336 are turned on. Thus, the first data bit DOUTMDQB_W is generated as the first path output signal MDQ_W by way of the NOR gate 314, the transmission gate 316, the latch 320, and the inverter 322, while the second data bit DOUTMDQB_X is generated as the second path output signal MDQ_X by way of the NOR gate 334, the transmission gate 336, the latch 340, and the inverter 342. As a result, the first and second data bits, DOUTMDQB_W and DOUTMDQB_X, are applied to the merged output generator 350 to output the merged output data bit DOUTMDQ.

In the SDR mode with the first burst type, the first and second single data rate signals, SDR_W and SDR_X, are set to low and high levels, respectively. The first and second transmission signals, W and X, are set to high and low levels, respectively. Thus, the first data bit DOUTMDQB_W triggers the first path output signal MDQ_W through the first path circuit 310. In the second path circuit 330, as the PMOS transistor 338 is turned on in response to the first single data rate signal SDR_W, which is at a low level, the node NB is charged up to a voltage of a high level. The node NB, which is at a high level sets the second path output signal MDQ_X to a high

level, which is then applied to the NAND gate 352 of the merged output signal generator 350 as an enable signal thereof. As a result, only the first data bit DOUTMDQB_W, of the two data bits, is provided to the merged output generator 350 and generated as the merged output data bit DOUTMDQ.

While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those skilled in the art that various modifications, additions and substitutions may be made therein without departing from the scope and spirit of the invention as described in the accompanying claims and their equivalents.